

REMARKS

In the Final Office Action dated November 28, 2005, claims 1-24 were pending, claims 1-17 and 24 were allowed, and claims 18-23 were rejected. In this response claims 18 and 21 are cancelled, therefore, claims 19-20 and 22-23 remain to be considered in this application. For the reasons set forth in detail below, applicant submits that the present application, including each of the pending claims is in condition for allowance.

Rejection Under 35 U.S.C. § 103(a) of Claims 18-23

In the Office Action, claims 18-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cecchi et al. (US Pat. No. 6,549,971) in view of Jeong et al. (US Pat. No. 5,675,584). Claims 18 and 21 are hereby cancelled.

The undersigned would like to thank the Examiner for the considered response and for the allowed claims. The present response merely brings a single issue to the Examiner's attention regarding claims 19-20 and 22-23, which, in large measure, was presented in the previous response dated September 28, 2005 and seems as though it may have been overlooked. The Examiner is respectfully invited to consider the following reasoning which demonstrates that Cecchi and Jeong, neither individually nor in combination, discloses the elements of claims 19-20 and 22-23.

Cecchi is directed to a system for amplifying a single differential signal and converting it into a single-ended signal. The system uses three differential amplifiers in two stages to amplify the signal to a communications receiver. The first stage uses two differential amplifiers to find the difference between the two polarities of the differential signal. The inputs to the amplifiers are reversed between the first and second differential amplifiers in this stage. This mechanism is used to balance out any inherent imbalances coming from differences in manufacture of the transistors. Common mode rejection in the differential amplifiers is controlled by feedback between different elements of the amplifiers. In the second stage of amplification, the output signals from the first stage are input into a third differential amplifier to produce a single-ended output signal.

Jeong is directed to a system for transmitting and receiving parallel data over a single serial line. The system converts outgoing parallel data to serial form and transmits it over a single serial line. It uses a two-way buffer to separate the incoming signal by subtracting the outgoing signal from the combined signal on the transmission line. The received data is then converted into parallel form and forwarded to the receiver.

In contrast, claims 19 and 22-23 are, *inter alia*, directed to methods and computer readable medium for providing bidirectional communication interface that comprises a bi-directional buffer, and wherein the buffer includes a differential amplifier that generates an output logic signal from a differential signal and filters out input noise by introducing asymmetry into the transfer characteristic. For example, where the transfer function for such a differential amplifier is centered around zero voltage, the transfer function will be centered around some other voltage, either greater or less than zero. The skewed transfer function then filters out input noise that is less than the size of the skew. The system uses this asymmetry in the transfer characteristic to avoid interpreting system noise as data.

Cecchi teaches away from the Applicant's use of asymmetry/skew. Cecchi, in col. 7, lines 17-20, describes the system as intended to compensate for the problems caused by asymmetry and recites "the parallel combination of first amplification stage 100 and second amplification stage 200 compensates for any asymmetries inherent in the amplification stages". In particular, the system in Cecchi helps to compensate for asymmetries that arise from "mismatch of the effective channel lengths or saturated drain currents of the p-channel and n-channel devices in each amplification circuit." Hence, Cecchi describes asymmetry/skew as a problem to be overcome. This is distinct from independent claims 19 and 22-23, which instead use asymmetry as a tool to eliminate the problem of input noise. For example claim 19 and 23 recite "suppressing effects of input noise on the output logic signals by skewing an output amplifier transfer characteristic", and claim 22 recites "suppressing effects of input noise from a floating input on the output logic signal by skewing a transfer characteristic of an output amplifier".

Jeong also fails to cure deficiencies of Cecchi. A *prima facie* case of obviousness under 35 U.S.C. § 103 requires, *inter alia*, a suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings (MPEP 2142). However, as described above, neither Cecchi nor Jeong, individually or in combination, discloses the elements of the rejected claims and therefore cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Therefore, the undersigned respectfully submits that independent claims 19 and 22-23, which include "suppressing effects of input noise on the output logic signals by skewing an output amplifier transfer characteristic," and dependent claim 20 are patentable over Cecchi and Jeong at least for the reasons above, and respectfully request the rejections be withdrawn.


Conclusion

In view of the foregoing, all of the claims pending in the application are in condition for allowance and, therefore, a Notice of Allowance is respectfully requested. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-3599.

Applicants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 120148004US3 from which the undersigned is authorized to draw.

Dated: 1/5/06

Respectfully submitted,

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